REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

Before addressing the specific rejections of record in this case, applicants have amended FIGS. 1 and 2 by extending the junction 35 though layers 32 and 14 as is described in the specification at paragraph [0055]. Stipulating has been added to the first semiconductor layer 14 in both of FIGS 1 and 2 as well. No other amendments have been made to FIGS. 1 and 2.

In the present Office Action, Claims 1-9 stand rejected under 35 U.S.C. § 112, second paragraph as allegedly indefinite. Specifically, the Examiner has alleged that applicants' use of the term "junction" in Claim 1 is improper. The Examiner has also pointed out that in Claim 1, lines 9-10 the use of the phrase "a first semiconductor layer" is confusing since a first semiconductor layer has been previously recited in the claims.

In response to the indefiniteness rejection, applicants submit that the term "junction" is properly used since it represents a meeting point of two differently doped semiconductor layers. Specifically, a junction 35 is formed as shown in FIGS. 1 and 2 between portions of the first semiconductor layer 14 and portions of the second semiconductor layer 34. The junction line 35 is shown passing through the second buried oxide layer 32 so as to indicate that the junction within the upper region is the same as the junction within the bottom region of the illustrated structures. Applicants observe that paragraph [0052] of the present application clearly discusses where and how the junctions are formed.

With respect to the term "a first semiconductor layer" found in Claim 1, lines 9-10, applicants have amended the same to read "said first semiconductor layer".

Applicants have also amended Claim 1 to positively recite that the claimed isolation region 30 provides lateral separation between the elevated device region 16 and the recessed device region 18. Support for this amendment to Claim 1 is found in FIGS. 1 and 2.

Applicants respectfully submit that the above remarks and amendments obviate the indefiniteness rejection raised in the present Office Action. Thus, reconsideration and withdrawal of the indefiniteness rejection are thus respectfully requested.

Claims 1 and 3-7 stand rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 6,424,020 to Vu, et al. ("Vu, et al."). Claim 2 stands rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Vu, et al. and U.S. Patent No. 5,482,871 to Pollack ("Pollack"). Claims 8 and 9 stand rejected under 35 U.S.C. § 103 as allegedly unaptentable over the combined disclosures of Vu, et al., and U.S. Patent No. 4,933,298 to Hasegawa ("Hasegawa").

Concerning the § 102(b) rejection, it is axiomatic that anticipation under § 102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants respectfully submit that Claims 1 and 3-7 are not anticipated by the disclosure of Vu, et al. since the applied reference does not disclose applicants' claimed SOI MOSFET structure of Claim 1. Specifically, Vu, et al. do not disclose an SOI MOSFET structure which

includes an elevated device region having at least one semiconductor device located on a second semiconductor layer, wherein said elevated device region further comprises a *source/drain junction which extends through the second semiconductor layer to an underlying first buried insulator layer, said first buried insulator is separated from the second semiconductor layer by a first semiconductor layer and a second buried insulator layer*; a recessed device region having at least one semiconductor device located atop said first semiconductor layer which is located on an upper surface of the first buried insulator; and *an isolation region laterally separating said elevated device region from said recessed device region.* Applicants submit that in the claimed structure the source/drain junction in the elevated device region extends through a second semiconductor layer 34, an underlying second buried insulating layer 32 and an underlying first semiconductor layer 14 to an underlying first buried insulating layer 14.

Vu, et al. provide a method of forming integrated circuitry of higher density and complexity than which can be obtained by using conventional multi-chip modules. Specifically, Vu, et al. provide a method for fabricating complex hybrid multi-functional circuitry having a common module body using at least one Si thin film transfer process to remove areas or tiles of circuitry formed in the Si films and transferring, locating and adhering the removed tiles to a common module body. Applicants observe that in the present Office Action the Examiner alleges that FIG. 17D anticipates the claimed structure. Applicants respectfully disagree since FIG. 17D does not include an elevated device region that comprises a *source/drain junction which extends through a second semiconductor layer to an underlying first buried insulator layer, said first buried insulator is separated from the second semiconductor layer by a first semiconductor layer and a second buried insulator layer*; a recessed device region having at least one semiconductor device located atop said first semiconductor layer which is located on an

upper surface of the first buried insulator; and *an isolation region laterally separating said elevated device region from said recessed device region.* Prior art FIG. 17D includes an elevated device region (p-channel device 1212) located atop a lower device region (n-channel device 1200). The two device regions are vertically separated by an insulating layer 1226. The elevated device region includes source/drain regions 1214 and a channel beneath the gate. The lower device region includes source/drain regions 1202 and a channel beneath the gate. The applied reference does not discloses that the elevated device includes a *source/drain junction which extends through a second semiconductor layer to an underlying first buried insulator layer, said first buried insulator is separated from the second semiconductor layer by a first semiconductor layer and a second buried insulator layer,* as presently claimed. Applicants further observe that in Vu, et al. the isolation region vertically separates the two different device regions, while in the claimed invention that device regions are laterally separated from each other.

The foregoing remarks clearly demonstrate that the applied reference does not teach each and every aspect of the claimed invention, as required by King and Kloster Speedsteel; therefore the claims of the present application are not anticipated by the disclosure of Vu, et al. Applicants respectfully submit that the instant § 102 rejection has been obviated and withdrawal thereof is respectfully requested.

With respect to the § 103 rejections, applications submit that the various combinations of applied prior art references, as cited in the present Office Action, do not render the claims of the present invention obviousness. Specifically, none of the applied prior art reference teach or suggest a structure which includes an elevated device region having at least one semiconductor device located on a second semiconductor layer, wherein said elevated device region further comprises a *source/drain junction which extends through the second semiconductor layer to an*

underlying first buried insulator layer, said first buried insulator is separated from the second semiconductor layer by a first semiconductor layer and a second buried insulator layer; a recessed device region having at least one semiconductor device located atop said first semiconductor layer which is located on an upper surface of the first buried insulator; and *an isolation region laterally separating said elevated device region from said recessed device region.* Applicants submit that in the claimed structure the source/drain junction in the elevated device region extends through a second semiconductor layer 34, an underlying second buried insulating layer 32 and an underlying first semiconductor layer 14 to an underlying first buried insulating layer 14 as presently claimed.

The principal reference spurring each of the obviousness rejections, i.e., Vu, et al., is defective for the same reasons as mentioned above in regard to the anticipation rejection. Applicants thus incorporate the above remarks concerning Vu, et al. herein by reference. To reiterate: Vu, et al. do not teach or suggest a structure including an elevated device region having a *source/drain junction which extends through a second semiconductor layer to an underlying first buried insulator layer, said first buried insulator is separated from the second semiconductor layer by a first semiconductor layer and a second buried insulator layer.* Vu, et al. also do not teach or suggest that that elevated device region is laterally isolated from the recessed device region, as presently claimed.

Pollack does not alleviate the above defects in Vu, et al since the applied secondary reference also does not teach or suggest the claimed structure having the features recited in Claim 1 of the present application. Pollack does not teach or suggest an elevated device region that has the claimed source/drain junction, nor that the elevated device region is laterally isolated from a recessed device region, as are presently claimed. Pollack provides a method of forming a

mesa-isolated SOI transistor using a split process polysilicon gate that includes the steps of depositing a buried oxide 14 on a Si substrate 12, depositing an SOI layer 16 on the buried oxide 14, and forming a gate oxide 18 on the SOI layer 16. The features of the claimed invention recited in Claim 1 of the present application are not disclosed or suggested in Pollack. Applicants note that Pollack is far removed from the claimed invention as evident by the Examiner's reliance of the disclosure of Pollack for teaching self-aligned junctions.

Hasegawa also does not alleviate the above defects in Vu, et al since the applied secondary reference also does not teach or suggest the claimed structure having the features recited in Claim 1 of the present application. Hasegawa provides a CMOS SOI structure that is fabricated by first forming an insulating SiO_2 layer on a Si substrate having a (100) plane. Openings are the formed in the SiO_2 layer to partially expose the Si substrate and polycrystalline or amorphous Si is then deposited on the SiO_2 and in the openings. The deposited silicon layer is divided into islands so that a first island includes one of the openings and a second island does not include any openings. A laser beam is then irradiated onto the islands so as to melt the islands, and when the laser light irradiation is discontinued, the melted islands recrystallize so that the first island forms a (110) plane and the second island forms a (100) plane. A p-channel MOSFET is fabricated on the first island, and an n-channel MOSFET is fabricated on the second island. The thus paired CMOS operates at high speeds, because the p-channel MOSFET using positive holes as the carrier is fast in a (110) crystal, and the n-channel MOSFET using electrons as the carrier is fast in a (100) crystal. The features of the claimed invention recited in Claim 1 of the present application are not disclosed or suggested in Hasegawa. Applicants note that Hasegawa is far removed from the claimed invention as evident by the Examiner's reliance of

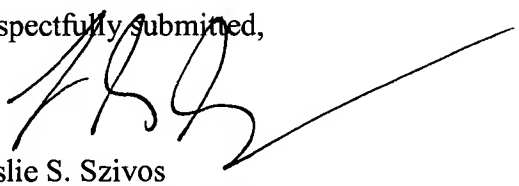
the disclosure of Pollack for teaching the feature recited in dependent Claims 8 and 9 of the present application.

The § 103 rejections also fail because there is no motivation in the applied references which suggest modifying the disclosed structures to include the claimed features of the present invention. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. § 103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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AMENDMENTS TO THE DRAWINGS:

The attached sheets of drawings include changes to FIGS. 1 and 2. These sheets, which include FIGS. 1 and 2, replace the original sheets including FIGS. 1 and 2.

Attachment: Replacement Sheets